



Connecting minds. Advancing light.

SPIE is the international society
for optics and photonics

SEARCH:

SEARCH

Conferences & Exhibitions Calendar

PRINT PAGE | E-MAIL PAGE | BOOKMARK



21 - 25 February 2010
San Jose Convention Center
San Jose, California, USA

Onsite News

On this page:

- [Thursday 25 February](#)
- [Wednesday 24 February](#)
- [Tuesday 23 February](#)
- [Monday 22 February](#)

The [Photo Gallery](#) highlights technical events, the Exhibition, and more.

The [Mock Trial Photo Gallery](#) provides coverage of judges, wigs, and much more.



Thursday 25 February 2010

It's back: Energy returns to lithography

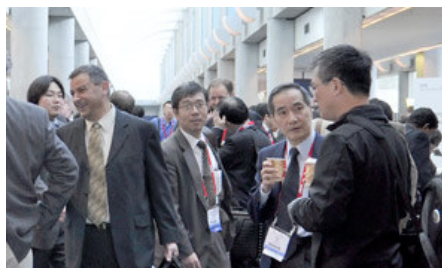
It was clear throughout SPIE Advanced Lithography that energy has returned to the lithography sector, agreed Symposium Chairs **Christopher Progler** and **Donis Flagello**. They praised the outstanding work on the part of conference chairs in organizing the programs, and the high-quality of content presented by the authors.

The week was characterized by full conference rooms, busy exhibit aisles, and networking that started over breakfast and continued long past dusk. Technical conference attendance was another indicator, coming in nearly one-third higher than last year. The final count for total attendance for 2010 was 2,100.

Standing-room-only conference rooms and high-energy networking continued through the final day, with the last sessions in five conferences, professional development courses, and award announcements topping off the week.

Andrew Estroff,

Rochester Institute of Technology, was given the Cymer-sponsored Best Student Paper in Optical Metrology Award for his paper on "Metamaterials for enhancement of DUV lithography." **Marshall Miller**, Univ. California, Berkeley,



won Honorary Mention for his paper on "Automatic numerical determination of lateral influence functions for fast CAD."

Technical special events concluded with a panel discussion on reference metrology in the nanotechnology process. The panel was moderated by **Vladimir Ukraintsev**, and included six panelists from Asia, Europe, and North America representing industry, academia, research, and manufacturing perspectives. Held in the Metrology, Inspection, and Process Control conference, the panel was also a part of the Global Collaboration in Reference Metrology working group meeting.

Wednesday 24 February 2010

Full rooms, busy aisles

All six conferences were in session on Wednesday, with many papers drawing packed audiences. Technical attendance is up more than 25% at this year's SPIE Advanced Lithography, reflecting an optimistic trend throughout the industry.

Technical special events included a panel sponsored by NIST on "Strategies for increasing the value of metrology and inspection," and a well-attended poster session for conferences on EUV, Alternative Technologies, Optical Microlithography, and Design for Manufacturability through DPI. Moderators for the NIST panel were **George Orji** and **Ronald Dixson**.

On Day Two in the exhibition hall, the aisles were full of shoppers and customers,

and exhibitors reported much deal making on the floor as well as at the numerous company events. "Based on AL and other indicators, 2010 looks better," said **Sara Eideh** of Synopsys. "We are delighted with how good Advanced Lithography 2010 has been." Eideh said turnout for her company was nearly 50% better than last year.



Tuesday 23 February 2010

Panel Discussions Address Nano and EUV

SPIE Advanced Lithography continues to be the place to find the right people, according to Day One feedback from exhibitors, with the steady traffic and strong energy on the exhibit floor providing more positive indicators of economic health. In the words of **Wilma Koolen-Hermken**, CEO of HamaTech, "It is obvious by the success of the meeting that the industry has begun to turn around."

Others were enthusiastic as well. "Advanced Lithography is awesome, as always," said **Ron Synowicki** of J.A. Woollam, who was already pleased with the leads he had gotten only four hours into the show. "Nothing is better than face-to-face interaction with customers. We're seeing a great mix of academia and industry."

"We were delighted that the attendees came in for afternoon coffee and stayed to talk business," said **Patti Shaw** of Brewer Science. "Leads are up over last year and the quality is good." Shaw said that Brewer doubled the number of staff they brought to Advanced Lithography this year, another indicator that business is on an up-swing.

Conference rooms were busy throughout the day and at times standing-room-only, and a panel on metrology in the current economy closed the day for the Metrology, Inspection, and Process Control conference.

A Women in Optics luncheon presentation featured a talk by **Anna Sidana** of One Million Lights, an initiative to improve education, personal income, health, and environmental quality in developing countries by replacing kerosene lamps with portable solar lighting.

It was a busy evening as well, with approximately 1,000 attendees at the

first of the week's two poster sessions, and a spirited "trial" pitting EUV against DPT.

Mock Trial Examines Rival Technologies

Only at SPIE Advanced Lithography in San Jose will you witness the world's top minds in the semiconductor industry donning black robes and white wigs and participating in a mock trial (heavy on the "mock") to determine the feasibility of rival technologies for the 22-nm HP node and beyond.

Like a scene from *Inherit the Wind* or *To Kill a Mockingbird*

seen through psychedelic lenses, an overflowing courtroom brimming with standing observers rose to honor Judges

Chris Progler of Photonics and **Donis Flagello** of Nikon as they entered the court. Representing EUVL were **Obert Wood** and **Bruno La Fontaine** of Global Foundries, and representing double patterning ArF were **Will Conley** of Freescale and **Mircea Dusa** of ASML.



Judges Chris Progler (left) and Donis Flagello

The judges encouraged the audience, who were serving as jury, to move to the side of the room they agreed with as the trial progressed. This would prove difficult, as all seats and all standing room was well occupied with rapt observers. Judge Flagello reiterated that this court observed no legal code other than Moore's Law, and as evidence of this, the jury was asked to stand and bow allegiance to a massive, projected image of Gordon Moore.

Opening arguments began with the case for EUVL, argued by Wood, who asserted that "it's all about k1." Comparing EUV vs DPL 193i, he showed significant degradation in DPL vs EUVL at 40-nm HP, and claimed that 22-nm HP was simply not possible with double patterning, while Zeiss had optical designs already to extend EUVL to below 22 nm.

Conley went on the attack in his opening arguments for double patterning, showing roadmaps of ArF pitch division vs EUV.

As a first witness, **Skip Miller** of ASML presented his cost analysis for patterning options at 2x-nm HP, showing that single-exposure EUV displayed the lowest cost of all options.

Tatsuhiko Higashiki of Toshiba showed the Toshiba roadmap for EUVL to extend the spacer process, declaring that a 2x-nm HP node process study will begin this year or next to address some primary challenge, such as defectively < 0.1/cm² and throughput above 100 wph.



From left, Nigel Farrar, Tatsuhiko Higashiki, Janice Golda, Paul Ackmann, and Skip Miller

Janice Golda then showed Intel's needs to ramp up manufacturing at the 22-nm node by 2015. For logic layouts, she said, one might need 4 or more masks. She also asserted that a microprocessor company like Intel is much more sensitive to mask defectively than a memory maker, so Intel was challenged to make a zero-defect EUV reticle, which they did accomplish recently.

Paul Ackmann from Global Foundries pointed out that the biggest issue is getting a new technology in place as soon as possible, and EUV has an advantage in that it can backfill to earlier technologies, while DPL cannot.

Nigel Ferrar of Cymer was asked whether EUVL could be powered without a

nuclear power plant, a reference to Burn Lin's oft-quoted assertion that EUVL sources will have exorbitant power needs. Ferrar stated that needs will be ~3x what an ArF scanner requires today, and that a 350 W source that delivers 150 wph will be available in 2011.

An energetic Conley then cross-examined the EUV team's witnesses on source power with a comedic figure of EUVL powered by the Hoover Dam, and plotted his estimation of EUV fab and tool costs vs the GDPs of countries like Tonga, Belize, and Latvia.

The witnesses for DPL then took the stand, beginning with **Kevin Lucas** of Synopsis, who showed multiple design rule and patterning options to extend into 22 nm and below.



From left, Kit Ausschnit, Andrew Hazelton, Patrick Wong, and Kevin Lucas

Kit Ausschnitt of IBM quoted Hamlet and displayed a very graphic animation of the "overlay elephant" that must be confronted to move to smaller nodes. He stated that overlay improvements will enable 193 nm DPL extension to 22 nm and beyond, but there will be no dearth of overlay challenges in either case. Certainly, he said, EUV is inevitable, but so is the imminent collapse of our sun. Possibly, he jabbed, EUVL will be ready by then.

Andrew Hazelton of Nikon then pointed to Nikon's S620D shown in the Plenaries to show that DP is available today, and **Patrick Wong** of IMEC showed that for the 22 nm node, various solutions show promise for different layers and applications.

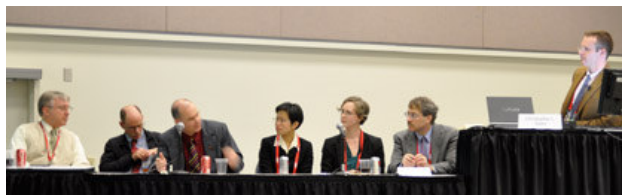
Wood's Perry-Masonesque cross-examination of the DPL witnesses focused on the cost issues and complexity of the many masks necessary. The DPL witnesses rebutted his math and stood their ground that overlay was not a problem for DPL.

After closing arguments, Judge Progler noted that the sheer number of observers serving as jurists made moving to their favored side of the room impossible, so he called for applause to determine the trial's winner. With equal applause, Progler declared a hung jury and adjourned, hinting that a retrial will be needed next year.

Many more photos are available in the [Mock Trial Photo Gallery](#).

Monday 22 February 2010

Panel Discussions Address Nano and EUV



Nanotechnology in Microlithography Panel Discussion: Self-Assembling Molecules for Semiconductor Patterning and Nanoelectronics

*Panel Moderators: **Richard M. Silver**, National Institute of Standards and Technology (United States) and **Christopher L. Soles**, NIST (United States)*

The evening panel discussion on nanotechnology in microlithography opened with comments by moderator Christopher Soles of NIST, who set the tone by contrasting "bottom-up" processes like self-assembly (SA) with traditional "top-down" lithographic processes. Between these technologies, Soles explained, we have major differences - natural shapes vs conventional circuit

design, local vs long-range order, monolayers vs high aspect ratio features, CMOS vs emerging applications, intrinsic scaling limits vs nanoscale dimensions, wet, soft processes vs clean room processes, slow ordering vs 100 wph, and the current pretty research pictures of SA vs true functional devices using lithography. He invited the panelists to discuss the near- and long-term prospects of SA and discuss the materials and metrology needs.

Dan Herr of SRC then presented some of the challenges of directed self-assembly, including the needed shapes, throughput, and defects. He asserted that SA could very well be an augmenting technology to current processes rather than a competing technology.

Greg Waldraff of IBM followed by presenting examples of electronic component self assembly on templated DNA biogrids, describing the ability of DNA origami to create nanoscale devices.

Lars Liebman, also of IBM, made a case for beginning research now at the NSF level so that the technology is mature by 2016-2017, the time period Herr had predicted SA could be introduced into manufacturing. However, he cautioned that the community needs to be sure it is tackling the right problem and not ignoring trimming or other issues.

Joy Cheng of IBM joined her colleague, Dan Herr, in displaying recent work in polymer self assembly, and Katy Bosworth predicted that the work they are doing at Hitachi on hard drive media could be one of the first to introduce block copolymers into a lithographic process.

Robert Brainard of Albany CNSE concluded the presentations by showing the relationship between chemically amplified resists, nanoimprint, and self assembly, asserting that each technology has great strengths but will not be replacing each other. The panel then opened for debate and questions from the audience.

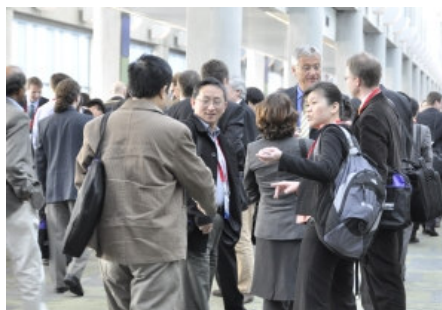


BACUS Technical Group Panel Discussion: EUV Source \$10M. EUV Scanner \$100M. Defect Free EUV Photomask, Priceless! For some there's NIL, for everyone else, there's EUV.

*Panel Moderators: **Bryan S. Kasprowicz**, Photronics, Inc.; **Franklin D. Kalk**, Toppan Photomasks, Inc. *Panel members (from left):* Gilroy Vandentop, Bryan Rice, Anthony Yen, Oliver Kienzle, Tatsuhiko Higashiki, Paul Ackmann, Ben Eynon.*

Advanced Lithography opens to optimism, overflowing house

A standing-room-only audience for the opening plenary session at SPIE Advanced Lithography in San Jose served as one more sign that the lithography industry is in a growth mode. Before the speakers from Nikon, Intel, and the venture capital firm Silver Lake Partners took the stage, a prestigious optical microlithography award and five new Fellows of SPIE were announced.



M. David Levenson, now associated with BetaSights, was named this year's winner of the Frits Zernike Award for Advances in Optical Microlithography, for his work in developing phase shifting masks. The Frits Zernike Award is sponsored by Cymer and ASML.

The five new Fellows from the lithography community -- **Robert Allen, Jon Benschop, Clifford Henderson, Soichi Owa**, and **James Potzick** -- are

among a total of 62 new Fellows of SPIE elected this year. The new Fellows were honored with 20 other lithography Fellows at a luncheon later in the day.

More awards followed the talks, including:

C. Grant Willson Best Paper award for 2009, to **Richard Lawson, Laren Tolbert,** and **Clifford Henderson** of Georgia Tech and **Todd Younkin** of Intel Corp.

Jeffrey Byers Award for Best Poster Paper in Resist Materials and Processing Technology for 2009, to **Xinyu Gu, Adam Berro, Younjin Cho, Kane Jen, Saul Lee, Tomoki Ngai, Toshiyuki Ogata, William Durand,** and **Grant Willson** of Univ. of Texas at Austin, **Arunkumar Sundaresan, Jeffrey Lancaster, Steffen Jockusch,** and **Nicholas Turro** of Columbia Univ., and **Paul Zimmerman** of Intel Corp.

The Willson award is sponsored by AZ Electronic Materials and Rohm Haas Electronic Materials, and the Byers award is sponsored by Tokyo Electron.

Three conferences opened sessions Monday morning, and two of several panel discussions scheduled for the week closed the day. Richard Silver and Christopher Soles of NIST moderated a panel on Self-Assembling Molecules for Semiconductor Patterning and Nanoelectronics. Bryan Kasproicz of Photronics Inc. and Franklin Kalk of Toppan Photomasks moderated the BACUS panel on future potential technologies, including EUV, NIL, double patterning and direct wire.

Plenaries Explore Past and Future of Lithographic Technologies

The plenary session for the 35th year of this symposium got underway with three presentations exploring the past successes and future prospects of lithographic technologies.

Kazuo Ushida of Nikon presented his predictions for lithography's future, promising not to bring bad news, because as the Japanese proverb goes, "The priest who preaches foul doctrine shall be reborn as a fungus." He predicted that although the next few years look good for fab equipment, it's very unlikely that this industry will return to its former levels. Current thought, said Ushida, is that double patterning will take lithography from the 32 to the 22-nm node, and EUV will take it from the 22 to the 16 nm node. However - what, he asked, if EUV comes too late? While the prospects of EUV are great for advancing to the 22-nm node, Ushida declared that EUV still has a long way to go because 100x improvement is required in mask defectivity to achieve such feature reduction. Should development of the necessary mask infrastructure start today, he predicted, it would take 2 years for tools to be available and another 2 years to fully understand defects before EUV could be a reality in 2014 - long after it would be needed for the 22-nm node. Because of this, one needs to look at alternative means of achieving the 22-nm node.

He presented three alternatives: spacer double patterning, pitch splitting double patterning, and line-cutting lithography, the last of which enables ArF extension to 16 nm. Because EUV is too far off to be practical, he said that 22 nm requires double patterning with immersion, which in turn will require high overlay accuracy, CD uniformity, excellent throughput, low cost of ownership, fast installation, and the possibility of reuse for next generations. He then presented Nikon's solution to all of these issues - the NSR-S620D - which has less than 2 nm overlay and 200 wph throughput and allows a modular approach to its construction enabling multigenerational use. Although 2010 and 2011 will be good years as the industry recovers, Ushida



Kazuo Ushida

asserted that EUV challenges in mask infrastructure will delay its implementation until the 16-nm node.

Eric Chen of Silver Lake Partners then gave an overview of the economics behind the lithography industry and voiced his concerns that without a change in global balances, the economy will never fully recover. However, he suggested that with a change in paradigms, there is great market potential. The root causes, he said, of the worst global economic conditions in recorded economic history (the 2009 recession) were the ease of liquidity, the US real estate market bubble, and the widespread excess leverage. These created a crisis that is just now seemingly stabilizing, but we aren't out of the woods yet. The last 20 years has seen an unprecedented integration of global economies that have resulted in an imbalance in the world economy. Chen asserted that this model is broken, and without normalized growth in developing economies as well as the driving down of debt and consumption in developed countries, the economy will not rebalance.



Eric Chen

Chen reminded the audience that a recession in the tech sector was seen most recently in 2000-2001 when the equity bubble burst (as opposed to 2009's debt bubble). Unfortunately, debt bubbles are more severe and harder to recover from. Two things drive economic growth - demographic changes and changes in productivity. Since productivity increases are driven by technology, Chen said, technology advances will likely save the day and drive new growth.

Chen then reviewed a number of macro trends in technology. First off, he described the evolution of software into a service economy, such as the change from CDs and personal programs to iPhone apps and cloud computing driving mobile and telecom. He pointed out the increasing pace and scale of clean technology, and then summarized the growing threat of Asia, noting its rise as an innovation leader as it moves from the inexpensive commercialization of technology to encompassing low-cost R & D on the leading end as well.

Sam Sivakumar of Intel then presented a talk that looked at the evolution of lithography as a play in four acts, starring the triumvirate of lithography, design, and process architecture.

In Act I: The Distant Past, Sivakumar considered the .25 micron and earlier technology and found that during that time period, lithography delivered design intent, but did not influence design or architecture. In Act II: The Recent Past (down to 65 nm), lithography then delivered design intent with some difficulty, such as in rule-based serif placement and hotspot determination. In present time, Act III (45-32 nm), lithography is now interacting closely with design and process architecture, profoundly influencing methodology in both areas.



Sam Sivakumar

As for the future, he predicted (1) lithography will play a central role in defining design methodology and process architecture; (2) mask technology has become and will continue to be an integral part of lithography planning for the next generation; and (3) managing the cost of patterning will be the real challenge in the near term. But lithography has become a full, equal partner with design and process integration and the quality of their interaction will determine the industry's success or failure.